

# HEF40175B

## Quad D-type flip-flop

Rev. 8 — 21 November 2011

Product data sheet

### 1. General description

The HEF40175B is a quad edge-triggered D-type flip-flop with four data inputs (D0 to D3), a clock input (CP), an overriding asynchronous master reset input ( $\overline{\text{MR}}$ ), four buffered outputs (Q0 to Q3), and four complementary buffered outputs ( $\overline{\text{Q0}}$  to  $\overline{\text{Q3}}$ ). Information on D0 to D3 is transferred to Q0 to Q3 on the LOW-to-HIGH transition of CP if  $\overline{\text{MR}}$  is HIGH. When LOW,  $\overline{\text{MR}}$  resets all flip-flops (Q0 to Q3 = LOW;  $\overline{\text{Q0}}$  to  $\overline{\text{Q3}}$  = HIGH), independent of CP and D0 to D3.

It operates over a recommended  $V_{\text{DD}}$  power supply range of 3 V to 15 V referenced to  $V_{\text{SS}}$  (usually ground). Unused inputs must be connected to  $V_{\text{DD}}$ ,  $V_{\text{SS}}$ , or another input.

### 2. Features and benefits

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$
- Complies with JEDEC standard JESD 13-B

### 3. Applications

- Shift registers
- Buffer/storage register
- Pattern generator

### 4. Ordering information

**Table 1. Ordering information**

All types operate from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$ .

Type number	Package		Version
	Name	Description	
HEF40175BP	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
HEF40175BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
HEF40175BTT	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1



### 5. Functional diagram

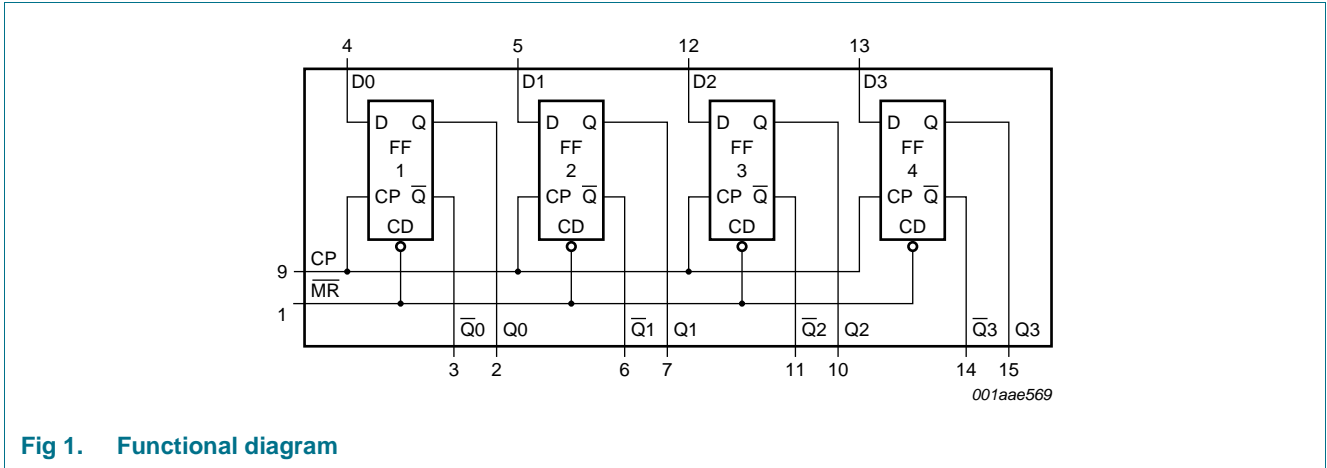


Fig 1. Functional diagram

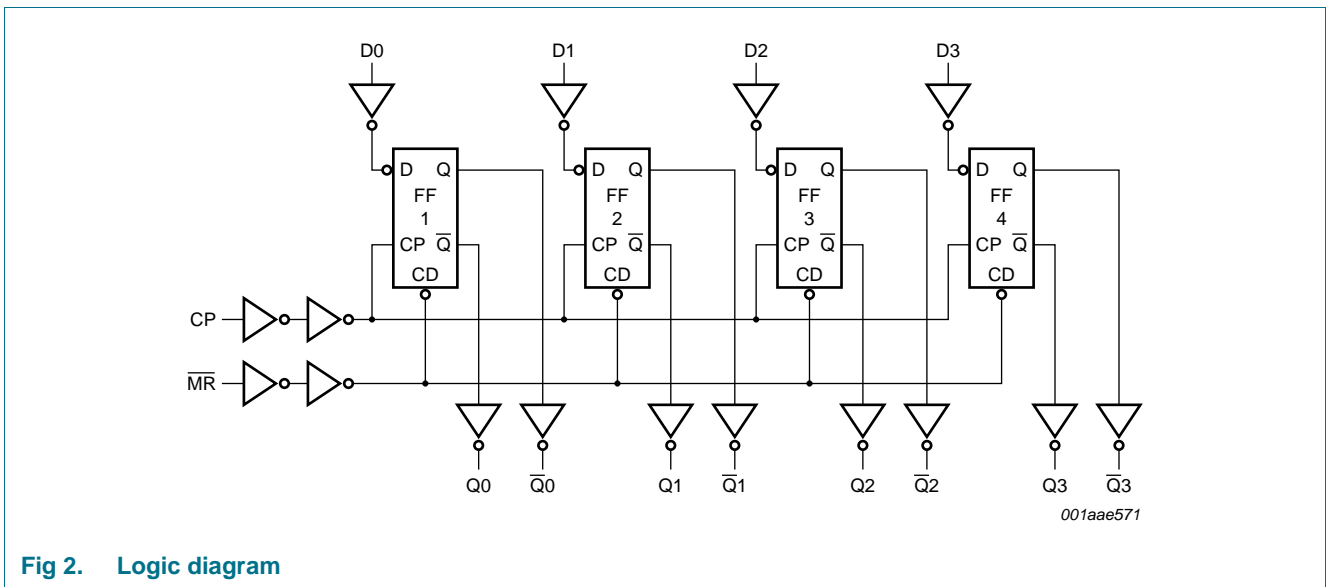
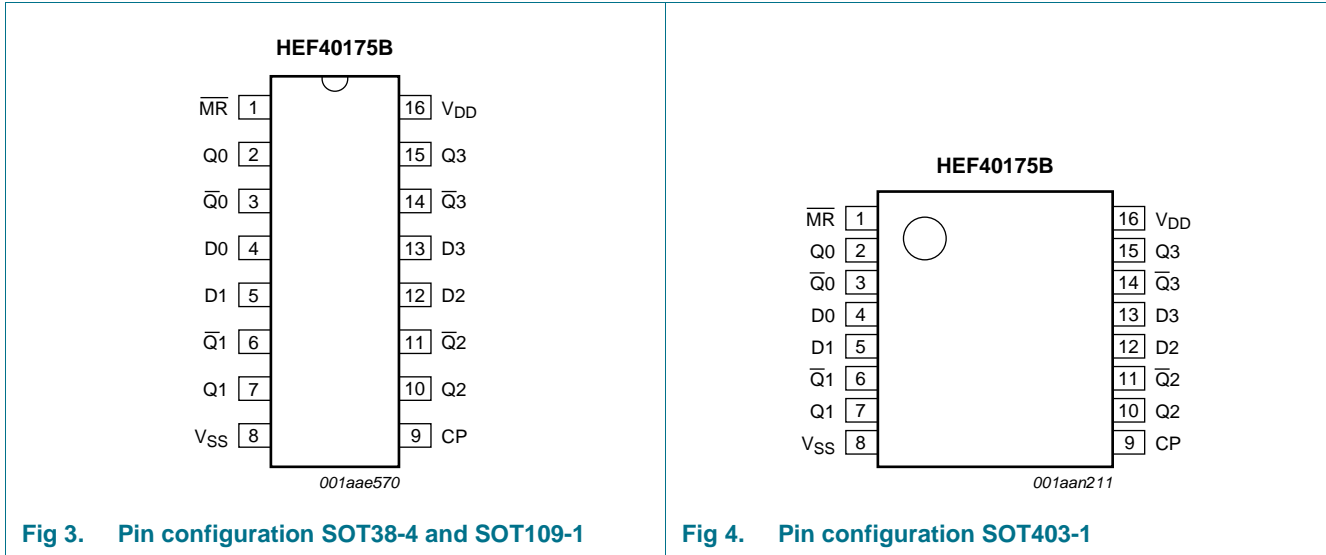


Fig 2. Logic diagram

## 6. Pinning information

### 6.1 Pinning



### 6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{\text{MR}}$	1	master reset input (active LOW)
Q0 to Q3	2, 7, 10, 15	buffered output
$\overline{\text{Q0}}$ to $\overline{\text{Q3}}$	3, 6, 11, 14	complementary buffered output
D0 to D3	4, 5, 12, 13	data input
VSS	8	ground supply voltage
CP	9	clock input (LOW-to-HIGH edge-triggered)
VDD	16	supply voltage

## 7. Functional description

Table 3. Function table [1]

Input			Output	
CP	Dn	$\overline{\text{MR}}$	Qn	Qn
↑	H	H	H	L
↑	L	H	L	H
↓	X	H	no change	no change
X	X	L	L	H

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = positive-going transition; ↓ = negative-going transition.

## 8. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage		-0.5	+18	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{DD} + 0.5\text{ V}$	-	$\pm 10$	mA
$V_I$	input voltage		-0.5	$V_{DD} + 0.5$	V
$I_{OK}$	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{DD} + 0.5\text{ V}$	-	$\pm 10$	mA
$I_{I/O}$	input/output current		-	$\pm 10$	mA
$I_{DD}$	supply current		-	50	mA
$T_{stg}$	storage temperature		-65	+150	°C
$T_{amb}$	ambient temperature		-40	+125	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$			
		DIP16 package	[1] -	750	mW
		SO16 package	[2] -	500	mW
		TSSOP16 package	[3] -	500	mW
$P$	power dissipation	per output	-	100	mW

[1] For DIP16 package:  $P_{tot}$  derates linearly with 12 mW/K above 70 °C.

[2] For SO16 package:  $P_{tot}$  derates linearly with 8 mW/K above 70 °C.

[3] For TSSOP16 package:  $P_{tot}$  derates linearly with 5.5 mW/K above 60 °C.

## 9. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD}$	supply voltage		3	-	15	V
$V_I$	input voltage		0	-	$V_{DD}$	V
$T_{amb}$	ambient temperature	in free air	-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5\text{ V}$	-	-	3.75	$\mu\text{s/V}$
		$V_{DD} = 10\text{ V}$	-	-	0.5	$\mu\text{s/V}$
		$V_{DD} = 15\text{ V}$	-	-	0.08	$\mu\text{s/V}$

## 10. Static characteristics

**Table 6. Static characteristics**

$V_{SS} = 0\text{ V}$ ;  $V_I = V_{SS}$  or  $V_{DD}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	$T_{amb} = -40\text{ }^{\circ}\text{C}$		$T_{amb} = +25\text{ }^{\circ}\text{C}$		$T_{amb} = +85\text{ }^{\circ}\text{C}$		$T_{amb} = +125\text{ }^{\circ}\text{C}$		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	3.5	-	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	11.0	-	V
$V_{IL}$	LOW-level input voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	-	1.5	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	-	4.0	V
$V_{OH}$	HIGH-level output voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	4.95	-	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	14.95	-	V
$V_{OL}$	LOW-level output voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	-	0.05	V
$I_{OH}$	HIGH-level output current	$V_O = 2.5\text{ V}$	5 V	-	-1.7	-	-1.4	-	-1.1	-	-1.1	mA
		$V_O = 4.6\text{ V}$	5 V	-	-0.64	-	-0.5	-	-0.36	-	-0.36	mA
		$V_O = 9.5\text{ V}$	10 V	-	-1.6	-	-1.3	-	-0.9	-	-0.9	mA
		$V_O = 13.5\text{ V}$	15 V	-	-4.2	-	-3.4	-	-2.4	-	-2.4	mA
$I_{OL}$	LOW-level output current	$V_O = 0.4\text{ V}$	5 V	0.64	-	0.5	-	0.36	-	0.36	-	mA
		$V_O = 0.5\text{ V}$	10 V	1.6	-	1.3	-	0.9	-	0.9	-	mA
		$V_O = 1.5\text{ V}$	15 V	4.2	-	3.4	-	2.4	-	2.4	-	mA
$I_I$	input leakage current		15 V	-	$\pm 0.1$	-	$\pm 0.1$	-	$\pm 1.0$	-	$\pm 1.0$	$\mu\text{A}$
$I_{DD}$	supply current	all valid input combinations; $ I_O  = 0\text{ A}$	5 V	-	1.0	-	1.0	-	30	-	30	$\mu\text{A}$
			10 V	-	2.0	-	2.0	-	60	-	60	$\mu\text{A}$
			15 V	-	4.0	-	4.0	-	120	-	120	$\mu\text{A}$
$C_I$	input capacitance		-	-	-	7.5	-	-	-	-	pF	

## 11. Dynamic characteristics

**Table 7. Dynamic characteristics**

$V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; for test circuit see [Figure 6](#); unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	Extrapolation formula	Min	Typ	Max	Unit
$t_{PHL}$	HIGH to LOW propagation delay	CP to $Q_n$ or $\overline{Q}_n$ ; see <a href="#">Figure 5</a>	5 V	$53\text{ ns} + (0.55\text{ ns/pF}) C_L$	-	80	160	ns
			10 V	$24\text{ ns} + (0.23\text{ ns/pF}) C_L$	-	35	70	ns
			15 V	$17\text{ ns} + (0.16\text{ ns/pF}) C_L$	-	25	50	ns
		$\overline{MR}$ to $Q_n$ ; see <a href="#">Figure 5</a>	5 V	$48\text{ ns} + (0.55\text{ ns/pF}) C_L$	-	75	155	ns
			10 V	$19\text{ ns} + (0.23\text{ ns/pF}) C_L$	-	30	65	ns
			15 V	$17\text{ ns} + (0.16\text{ ns/pF}) C_L$	-	25	50	ns

**Table 7. Dynamic characteristics ...continued**  
 $V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; for test circuit see [Figure 6](#); unless otherwise specified.

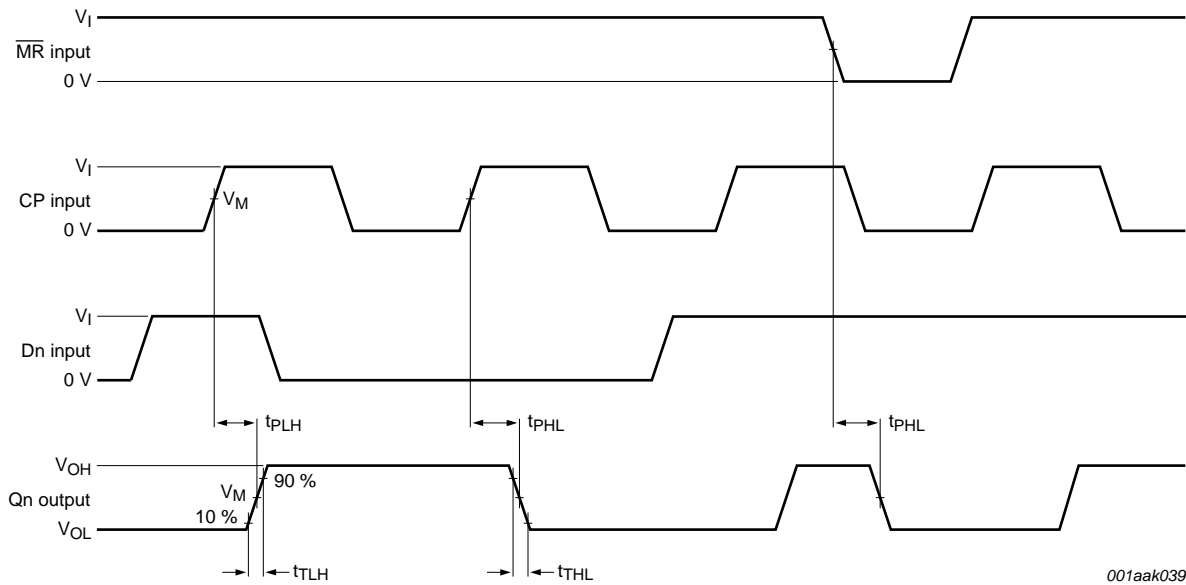
Symbol	Parameter	Conditions	$V_{DD}$	Extrapolation formula	Min	Typ	Max	Unit
$t_{PLH}$	LOW to HIGH propagation delay	CP to $Q_n$ or $\overline{Q}_n$ ; see <a href="#">Figure 5</a>	5 V	$43\text{ ns} + (0.55\text{ ns/pF}) C_L$	-	70	140	ns
			10 V	$19\text{ ns} + (0.23\text{ ns/pF}) C_L$	-	30	65	ns
			15 V	$17\text{ ns} + (0.16\text{ ns/pF}) C_L$	-	25	45	ns
		$\overline{MR}$ to $\overline{Q}_n$ ; see <a href="#">Figure 5</a>	5 V	$43\text{ ns} + (0.55\text{ ns/pF}) C_L$	-	70	140	ns
			10 V	$19\text{ ns} + (0.23\text{ ns/pF}) C_L$	-	30	65	ns
			15 V	$17\text{ ns} + (0.16\text{ ns/pF}) C_L$	-	25	50	ns
$t_t$	transition time	see <a href="#">Figure 5</a>	5 V	$10\text{ ns} + (1.00\text{ ns/pF}) C_L$	-	60	120	ns
			10 V	$9\text{ ns} + (0.42\text{ ns/pF}) C_L$	-	30	60	ns
			15 V	$6\text{ ns} + (0.28\text{ ns/pF}) C_L$	-	20	40	ns
$t_{su}$	set-up time	Dn to CP; see <a href="#">Figure 5</a>	5 V		60	30	-	ns
			10 V		20	10	-	ns
			15 V		15	5	-	ns
$t_h$	hold time	Dn to CP; see <a href="#">Figure 5</a>	5 V		+25	-5	-	ns
			10 V		10	0	-	ns
			15 V		10	0	-	ns
$t_w$	pulse width;	CP input LOW; minimum pulse width see <a href="#">Figure 5</a>	5 V		90	45	-	ns
			10 V		35	15	-	ns
			15 V		25	10	-	ns
		$\overline{MR}$ input LOW; minimum pulse width see <a href="#">Figure 5</a>	5 V		80	40	-	ns
			10 V		30	15	-	ns
			15 V		20	10	-	ns
$t_{rec}$	recovery time	$\overline{MR}$ input; see <a href="#">Figure 5</a>	5 V		0	-30	-	ns
			10 V		0	-20	-	ns
			15 V		0	-15	-	ns
$f_{max}$	maximum frequency		5 V		5	11	-	MHz
			10 V		15	30	-	MHz
			15 V		20	45	-	MHz

[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formula shown ( $C_L$  in pF).

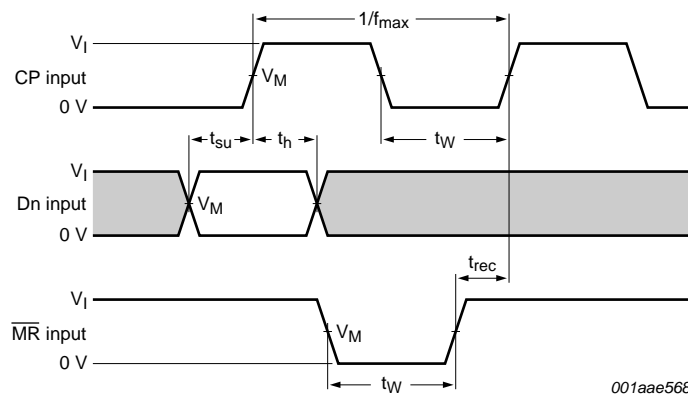
**Table 8. Dynamic power dissipation  $P_D$**   
 $P_D$  can be calculated from the formulas shown.  $V_{SS} = 0\text{ V}$ ;  $t_r = t_f \leq 20\text{ ns}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

Symbol	Parameter	$V_{DD}$	Typical formula for $P_D$ ( $\mu\text{W}$ )	where:
$P_D$	dynamic power dissipation	5 V	$P_D = 2000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	$f_i$ = input frequency in MHz, $f_o$ = output frequency in MHz, $C_L$ = output load capacitance in pF, $V_{DD}$ = supply voltage in V, $\Sigma(f_o \times C_L)$ = sum of the outputs.
		10 V	$P_D = 8400 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	
		15 V	$P_D = 22500 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	

12. Waveforms



a. CP and  $\overline{MR}$  to Qn Propagation delays and Qn transition times



b. Minimum pulse widths for CP and  $\overline{MR}$ ,  $\overline{MR}$  to CP recovery time, and set-up and hold time for Dn to CP

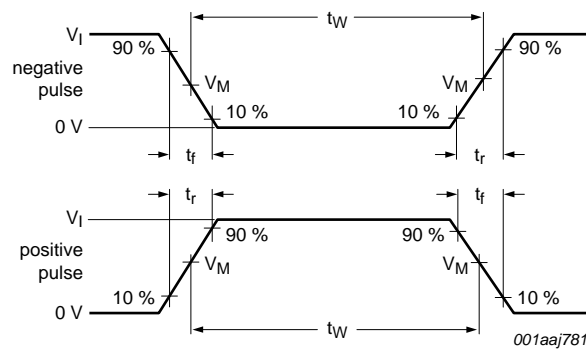
$V_{OH}$  and  $V_{OL}$  are typical output voltage levels that occur with the output load.

Set-up and hold times are shown as positive values but may be specified as negative values.

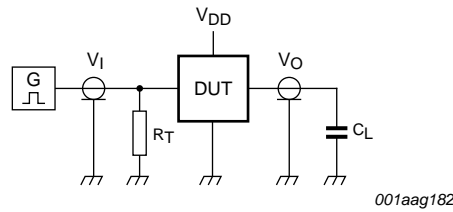
The shaded area are where input changes result in predicable output performance.

Measurement points are given in [Table 9](#).

Fig 5. Waveforms showing switching times



a. Input waveforms



b. Test circuit

Test and measurement data is given in [Table 9](#)

Definitions test circuit:

DUT = Device Under Test;

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator;

$C_L$  = Load capacitance including jig and probe capacitance.

Fig 6. Test circuit for measuring switching times

Table 9. Measurement points and test data

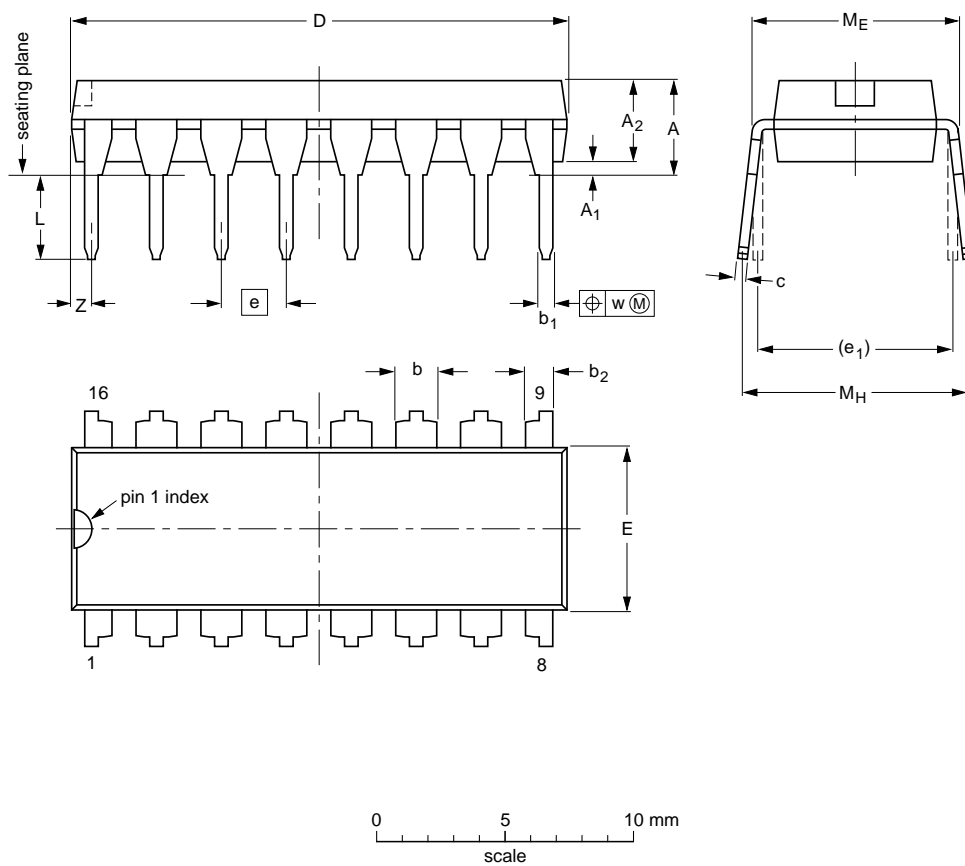
Supply voltage	Input	Load
$V_{DD}$	$V_I$	$C_L$
5 V to 15 V	$V_{SS}$ or $V_{DD}$	50 pF
		$t_r, t_f$
		$\leq 20$ ns



13. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	b <sub>2</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-4						95-01-14 03-02-13

Fig 7. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

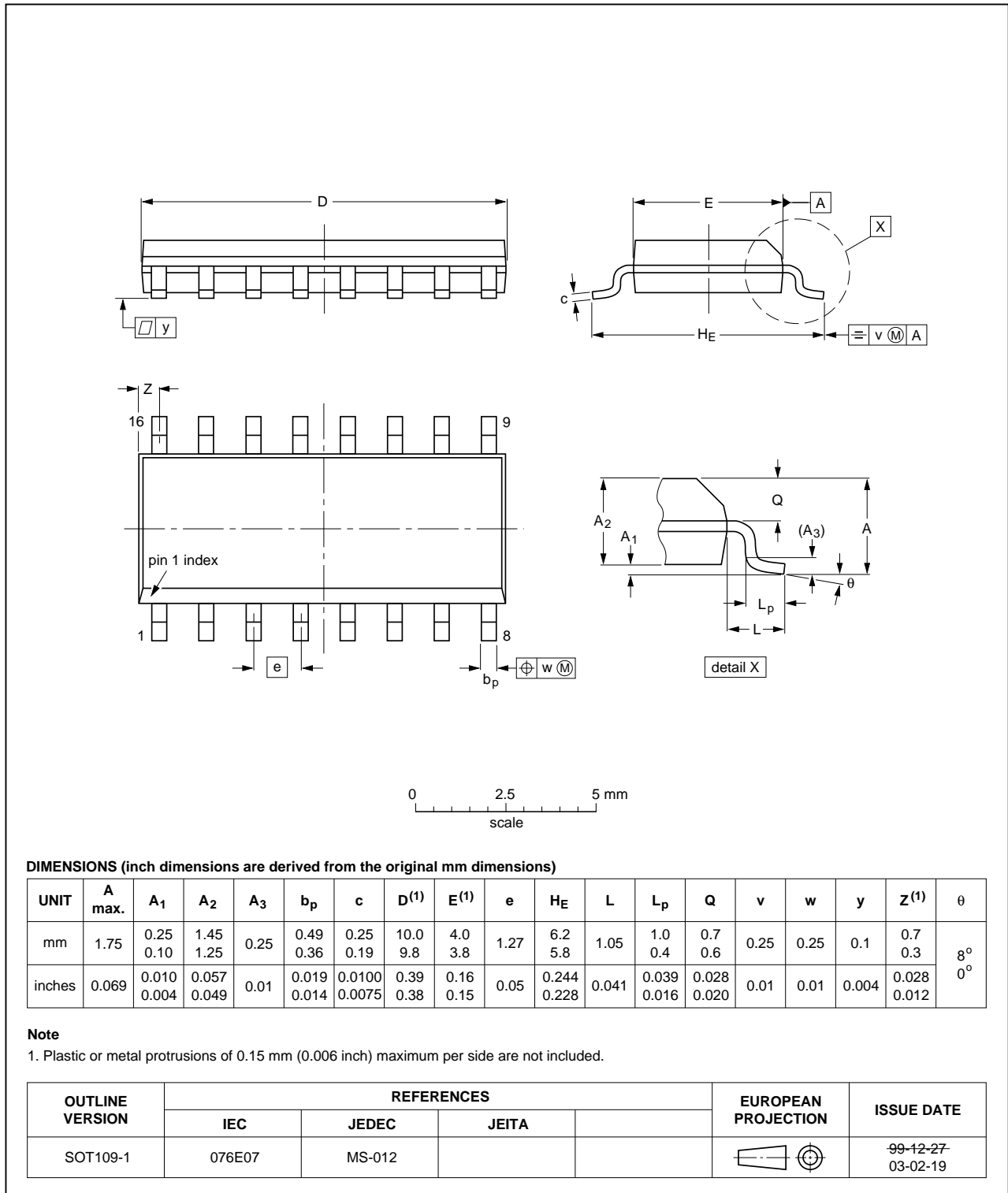


Fig 8. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

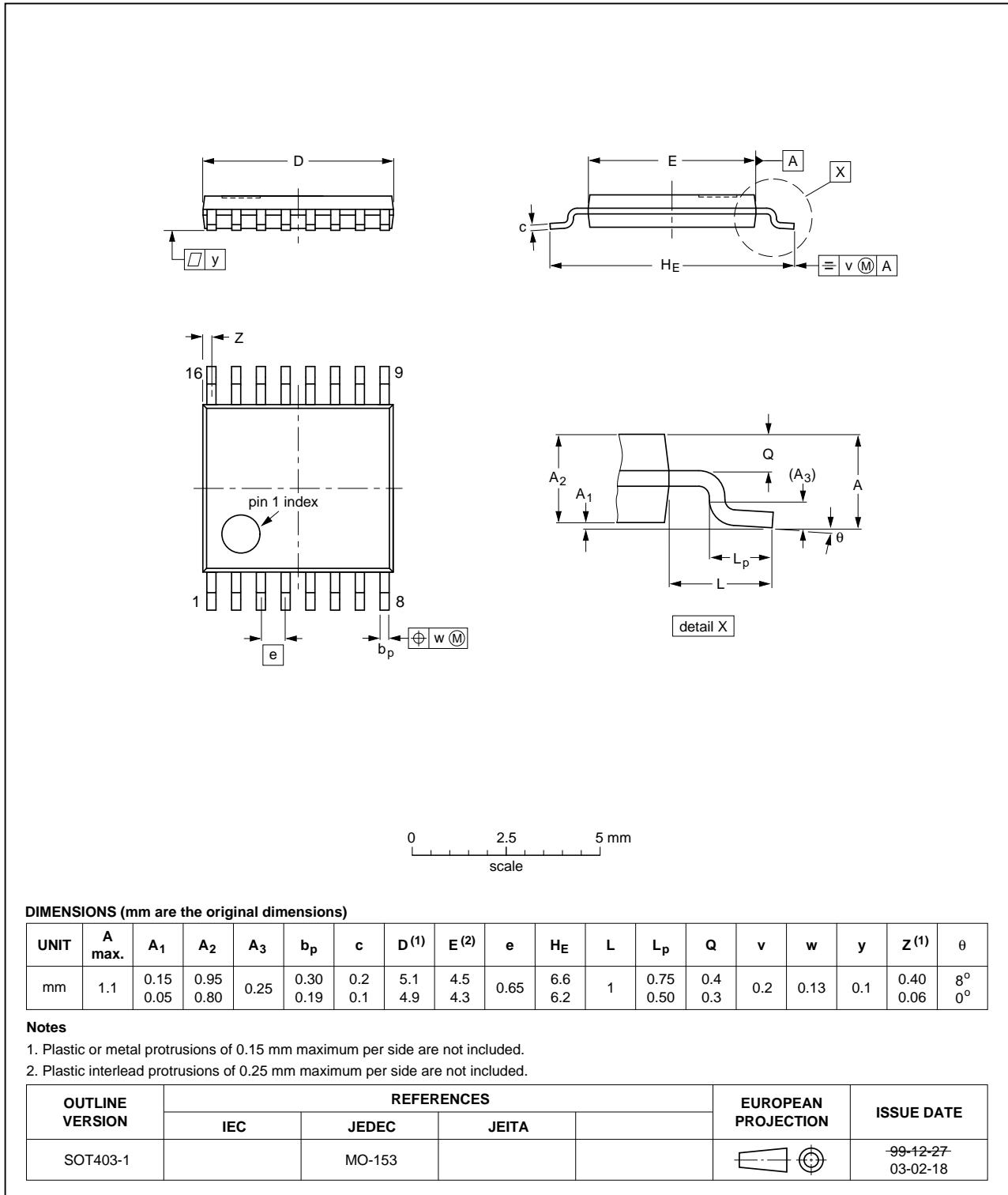


Fig 9. Package outline SOT403-1 (TSSOP16)

## 14. Revision history

**Table 10. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF40175B v.8	20111121	Product data sheet	-	HEF40175B v.7
Modifications:		<ul style="list-style-type: none"><li>• Legal pages updated.</li><li>• Changes in “General description”, “Features and benefits” and “Applications”.</li></ul>		
HEF40175B v.7	20110503	Product data sheet	-	HEF40175B v.6
HEF40175B v.6	20101214	Product data sheet	-	HEF40175B v.5
HEF40175B v.5	20100105	Product data sheet	-	HEF40175B v.4
HEF40175B v.4	20090813	Product data sheet	-	HEF40175B_CNV v.3
HEF40175B_CNV v.3	19950101	Product specification	-	HEF40175B_CNV v.2
HEF40175B_CNV v.2	19950101	Product specification	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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